HFA1100 Single 5V Supply Application

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Introduction

This application note discusses how to design a video amplifier circuit with gains ≥2 in a single 5V supply application using the HFA1100 video op amp.

Table 1 shows the typical performance data for the HFA1100. The two most important parameters that determine the design configuration are the Common Mode Input Range (CMIR) and the Output Voltage Swing. If either of these two parameters are violated then the rest of the data listed in this table would not necessarily be achieved.

The first circuit to be discussed (see Figure 1), biases the op amp input and output at 2.5V to take full advantage of the CMIR and the output swing capability of the HFA1100. In order to properly center the input of the op amp, C_1 is needed to AC couple the input to the amplifier circuit and a resistor divider is formed with R_2 and R_3 to bias the input at 2.5V. R_2 and R_3 were set to 5K in order to keep the bias current small (i.e., $I_{BIAS} = 5/(R_2 + R_3) = 0.5mA$). C_2 AC couples the negative input of the op amp such that the DC voltage at the op amp input sees a gain of 1 through the amplifier and the AC voltage sees a gain of $1+R_5/R_4$ at frequencies well above the roll-off frequency of C_2. If C_2 were not present, then the DC and AC gain would be equal to $1+R_5/R_4$; therefore, the output and input can't be centered unless the gain equals 1. As an example, if C_2 were not present and a gain of 5 were desired then the input bias voltage would have to be 0.5V in order to center the output at 2.5V. But this would violate the CMIR of the op amp which would degrade the op amps performance. Since the DC gain is 1 with C_2 present, this allows a large AC gain as long as the maximum output swing of the amplifier is not exceeded. The roll-off frequency for C_2 is determined by the equation $f = 1/(2*\pi*R_4*C)$, so for this circuit f = 3kHz. A couple of the drawbacks of this circuit are the offset voltage and low frequency noise contributed by the presence of R_2 and R_3. The output offset contribution from these resistors can be calculated from the equation $V_{OS(OUT)} = Ib*(R_2||R_3)*A_{VDC}$ where Ib is the bias current of the op amp and A_{VDC} is the DC gain.

For the circuit in Figure 1, $A_{VDC} = 1$, $R_2||R_3 = 2.5k\Omega$, and Ib is 25µA for the HFA1100 so $V_{OS(OUT)} = 63mV$. The output noise voltage contribution from $R_2||R_3$ can be calculated from the equation $Ip*(R_2||R_3)*A_{VAC}$ where Ip is the +Input noise current of the op amp. For the circuit shown in Figure 1, the output noise contribution from $R_2||R_3$ would be 90nV/sqrt(Hz).

To avoid the offset voltage and low frequency noise contributions from R_2 and R_3, the circuit in Figure 2 was developed. The operation of this circuit is essentially the same as Figure 1 except that the 2.5V bias voltage is supplied from a low output impedance DC supply. R_1 provides the 50Ω termination and C_2 provides a good AC ground at the power supply. The major benefit of using this circuit is the fact that R_1 provides a low impedance to ground which gets rid of the offset voltage and low frequency noise contributions that were seen in the other circuit. Shown in Figures 3 and 4 are the step response and the frequency response for the HFA1100 in the two circuits discussed above.

TABLE 1. HFA1100 SINGLE 5V PERFORMANCE DATA

PARAMETER	TYP
Input Common Mode Range	1V to 4V
-3dB BW (A_V = +2)	267MHz
Gain Flatness (to 50MHz, A_V = +2)	0.05dB
Output Voltage (A_V = -1)	1.3V to 3.8V
Slew Rate (A_V = +2)	475V/µs
0.1% Settling Time	17ns
Supply Current	5.5mA

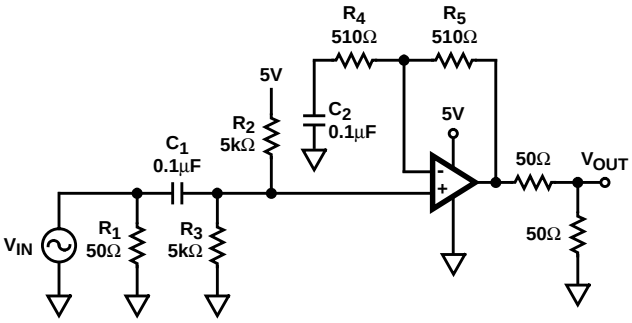

FIGURE 1. HFA1100 WITH A_V = +2 AND A HIGH SOURCE IMPEDANCE BIAS NETWORK

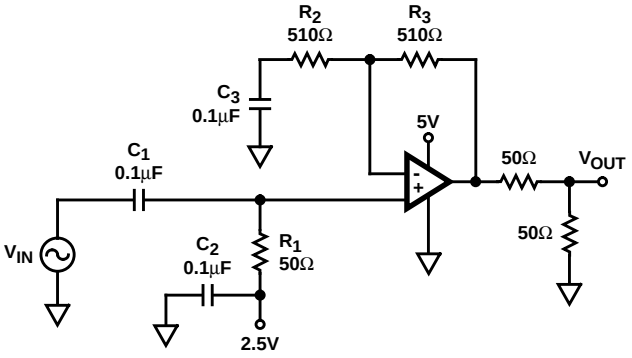

FIGURE 2. HFA1100 WITH A_V = +2 AND A LOW SOURCE IMPEDANCE BIAS NETWORK

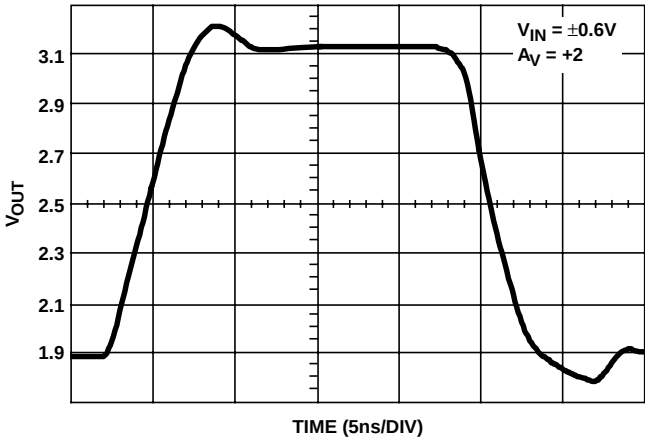

FIGURE 3. HFA1100 TRANSIENT RESPONSE FOR CIRCUITS IN FIGURES 1 AND 2

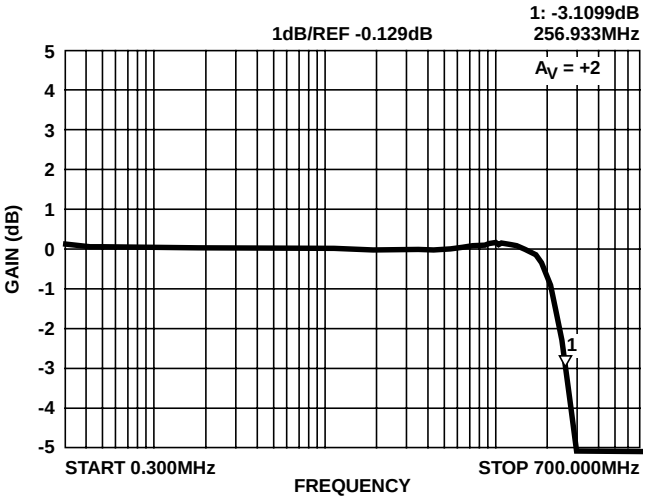

FIGURE 4. HFA1100 FREQUENCY RESPONSE FOR CIRCUITS IN FIGURES 1 AND 2

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